

**REMARKS**

Claims 1-6, 8-13, 15 and 20-23 are pending in the application. Claims 1-6 are withdrawn from consideration and claims 20-23 are newly added to the application.

**Claim Rejections under 35 USC §103**

Claims 8-13 and 15 are rejected under 35 USC §103(a) as being unpatentable over Harada et al. (U.S. Patent 6,417,575 B2) in view of Lee et al. (U.S. Patent 6,163,074).

The present invention is a semiconductor device having a pad capable of suppressing excess current concentration. As illustrated in Fig. 2a, the pad includes a large number of insulating regions (21a) in which specific ratios of dimensions are followed. For example, W1 corresponds to the width of the wiring portion (25). The pad is divided into three portions. A first frame area (27a) having a width of L1. A second frame area (27c) has a width L2 and contains several insulating regions (21a). A central area (27d) is contained in the middle of the pad and may contain a via hole. The width L1 of the first frame area (27 a) is equal to or wider than the distance between insulating regions (21a). As illustrated in Fig. 2A, the total width of pad (27) corresponds to  $2 \times W2 + n \times W3$  as discussed on page 11, line 22 of the specification, W1 correspond to the distance L1 and W3 corresponds to the distance P2. As discussed in the example provided on page 12, lines 4-11, W1 is larger than the distance L1 and the ratio  $L1/W1$  is 30 percent or higher.

Harada et al. describes a semiconductor device and method of manufacturing the same which includes a pad electrode and main electrode layer. This device includes a first interlayer insulating film (7) a first intra-layer insulating film (11).

Lee et al. describes a semiconductor device having a lower single-bodied conductive plug (930) and a lower island insulator (925I) as shown in figures 9 and 10. With this design a bonding pad having reduced cracking in an insulating layer is possible.

The Examiner states in lines 4-7 on page 3 of the office Action:

“Harada shows (fig. 77A) all the limitations of the claim 7 (claim 9?) The plurality of insulating regions (341) not disposed in a near wiring area superimposed upon an extended area of the wiring part into the pad part.”

For the Examiner's convenience, a copy of Figs. 77A and 77B of Harada is attached hereto.

In the copy, the lower protruding section 240 is labeled as yellow., the stress buffer metal layer 340 labeled as blue, the stress buffer insulating partition 341 is labeled as pink, and the wiring is labeled as green.

As shown in Figs. 77A and 77B attached herewith, the insulating film coupled with the stress buffer insulating partition 341 surrounds the lower protruding section 240. The insulating film continuous with the stress buffer insulating partition 341 is disposed in the near wiring area, which is indicated by hatching in the attached copy. Namely, an insulating region is disposed in the near wiring area. Therefore, Applicant believes the Examiner is incorrect.

Furthermore, with regard to Figs. 9, 10 and 18 of Lee, the Examiner states in lines 11-12 on page 3 of the Office Action, “the insulating regions (925 I) are disposed in a second frame area with

a first frame area only.” However, as shown in Figs. 8, 9 and 10 of Lee, insulating regions (925 I) are distributed uniformly in the pad area. The distribution of Lee’s insulating regions (925 I) is the same as that shown in Fig. 11 (Prior Art) of the present application. Lee’s device does not have an area corresponding to the near wiring area (27b) of claim 9, in which the insulating regions (21a) are not distributed. Also, in Lee’s device shown in Fig. 18, insulating regions (925 I) are distributed in an area adjacent to the outer periphery of the pad.

Therefore, even if Lee’s insulating regions (945 I) were distributed in Harada’s pad area, the near wiring area as defined in claim 9 could not be obtained.

Furthermore, in claim 9, the plurality of insulating regions, the first pad and the wiring are located in the same layer as the first intra-layer insulating film. In Figs. 77A and 77B of Harada attached hereto, the wiring is labeled as green. The wiring continuous with the conductive region 101 is clearly located in the layer different from the layer in which the lower protruding section, the stress buffer metal layer 340 and the stress buffer insulating partition 341 are located.

Claim 12 comprises the limitation that the width of the first frame area is wider than the pitch of insulating regions. Lee does not disclose a frame area, the width of which is wider than the pitch of the insulating regions (945 I).

**Conclusion**

In view of the aforementioned amendments and accompanying remarks, claims 9 and 15, are believed to be in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicant's undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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